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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,470	03/24/2004	Renfeng Gao	7033.0078	2916

39878            7590            04/12/2007  
MH2 TECHNOLOGY LAW GROUP  
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SUITE 550  
TYSONS CORNER, VA 22182

EXAMINER
ROJAS, OMAR R

ART UNIT	PAPER NUMBER
2874	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/807,470	GAO ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Omar Rojas	2874	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on \_\_\_\_\_.
- 2a) This action is **FINAL**.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-39 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-39 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 03/24/2004 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) Notice of Informal Patent Application
- 6) Other: Detailed Action.

## **DETAILED ACTION**

### ***Drawings***

1. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the line quality is not uniformly thick or well-defined. See 37 CFR 1.84(l). Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

### ***Specification***

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### ***Claim Objections***

3. Claim 15 is objected to because of the following informalities: In claim 15, the recited limitation "the photonic chip sub-mount" lacks a clear antecedent basis. Appropriate correction is required.

4. Claim 18 is objected to because of the following informalities: In claim 18, the recited limitation "the first alignment feature" lacks a clear antecedent basis. Appropriate correction is required.

5. Claim 21 is objected to because of the following informalities: In claim 21, the recited limitation "the second surface" lacks a clear antecedent basis. Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. **Claims 1-12, 14-16, 28-33, and 35-37 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Patent No. 5,319,725 to Buchmann et al. ("Buchmann").**

*In re* claims 1-6, 28, 29, and 32, Buchmann discloses an optical assembly (Figures 2-10)

comprising:

a first photonic/electronic/mechanical substrate/chip/chip sub-mount (10, 13, 40, 41, 60, and/or 64) comprising a first surface comprising at least a first structure/device/clipgate (11, 12, 14, 15, 42, and/or 41.1) and at least a first alignment feature/device/clipgate (11, 12, 14, 15, 42, and/or 41.1);

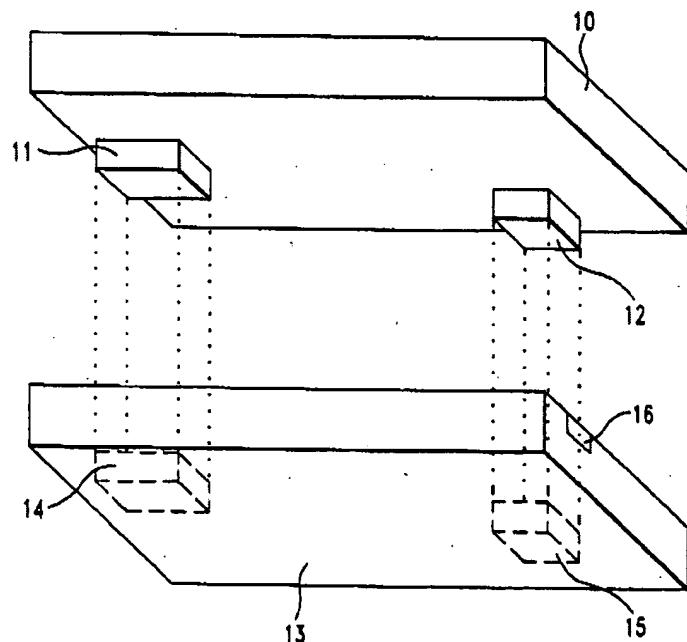
a second photonic/electronic/mechanical substrate/chip/chip sub-mount (10, 13, 40, 41, 60, and/or 64) comprising a first surface comprising at least a second structure/device/clipgate (11, 12, 14, 15, 42, and/or 41.1) complementary to each of the at least first structures and at least a second alignment structure/device/clipgate (11, 12, 14, 15, 42, and/or 41.1) complementary to each of the at least first alignment features; and

a device (11, 12, 14, 15, 16, 42, and/or 41.1) mounted to at least one of the first surface of the first substrate/chip/chip sub-mount and the first surface of the second substrate/chip/chip sub-

mount, the device selected from one of a photonic device, an electrical device, and a mechanical device;

wherein the first surface of the first chip (10, 13, 40, 41, 60, and/or 64) or chip sub-mount is in physical contact with the first surface of the second chip or chip sub-mount (10, 13, 40, 41, 60, and/or 64) such that each of the first alignment features and each of the corresponding second alignment features are in contact thereby permitting each of the at least first structures to be physically aligned with each of the corresponding complementary at least second structures (e.g., see column 7, lines 15-34);

wherein the chip (10, 13, 40, 41, 60, and/or 64) secures together with the chip sub-mount (10, 13, 40, 41, 60, and/or 64) (e.g., see column 7, lines 31-40). Figure 3 of Buchmann is reproduced below.



*In re* claims 7, 8, 30, 31, and 36, Buchmann discloses the particular limitations at column 7, line 65 to column 8, line 9.

*In re* claims 9-12, Buchmann further discloses rectangular or v-shaped trenches (14, 15, 66.1 and/or 70.1) and a photonic device (11, 12, 16, 62.1, 68.1 and/or 71.1) as claimed.

*In re* claim 14-16, the recited limitations are clearly shown Figures 3 and 6 of Buchmann.

*In re* claim 33, the recited limitations are disclosed by Buchmann at column 7, lines 37-41.

*In re* claim 35, the recited limitations are disclosed by Buchmann at column 7, lines 26-31.

*In re* claim 37, the recited limitations are disclosed by Buchmann at column 7, lines 17-21.

**8. Claims 17-19 and 21-23 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Patent No. 6,116,962 to Laity.**

*In re* claim 17, Laity discloses an optical assembly (Figures 1-10) comprising:

a first substrate 100 comprising a first surface 102 comprising a first device 108/112; and a second substrate 10 comprising a first surface 18 comprising a first recess 82, wherein a surface geometry of the first recess 82 of the second substrate 10 is complementary to the first surface 102 of the first substrate 100, and a second device 138/140/230/240, wherein contacting the first substrate 100 to the second substrate 10 permits the first surface 102 of the first substrate to fit into the first recess 82 of the second substrate 10 and permits the first device 108/112 to be aligned with the second device 138/140/230/240, and further wherein the first and second devices 138/140/230/240 are chosen from photonic devices, electrical devices, and mechanical devices. Figures 1 and 10 of Laity are reproduced below.

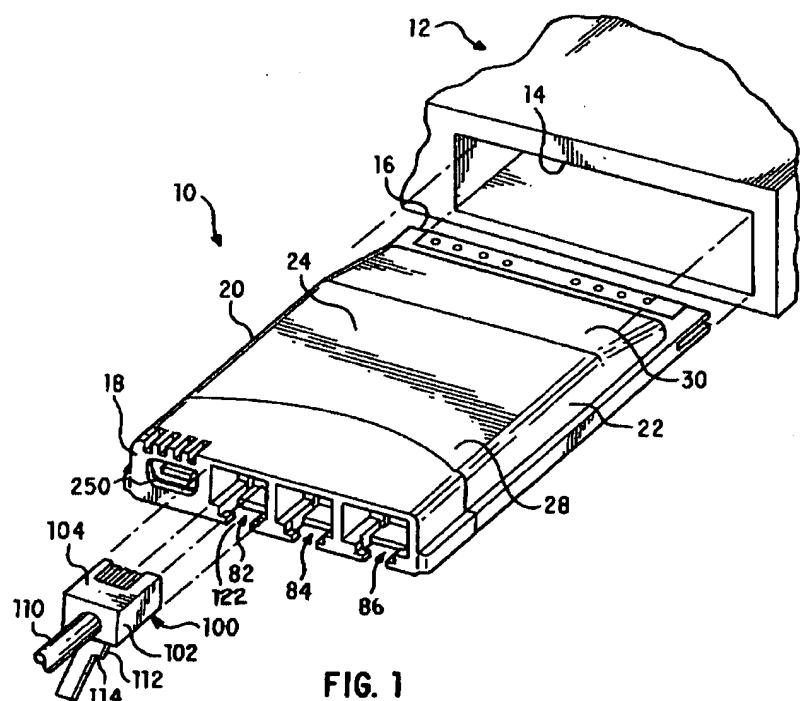


FIG. 1

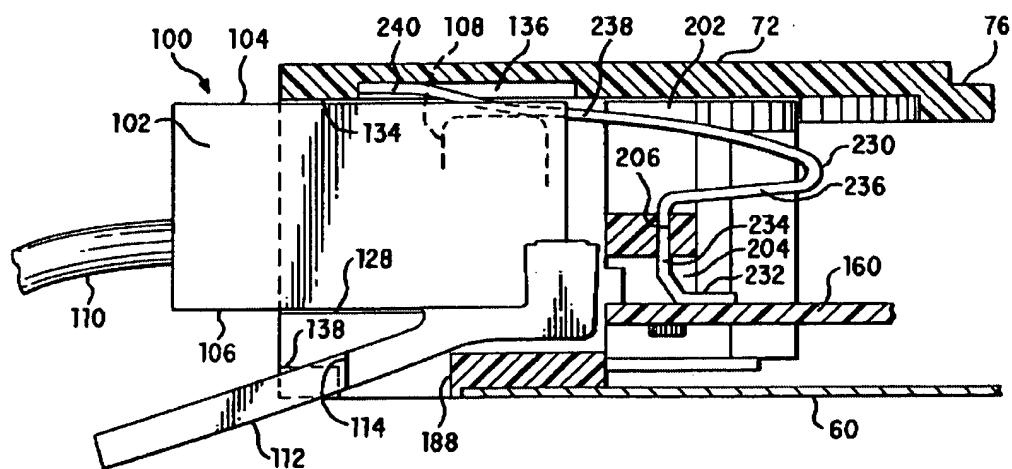


FIG. 10

*In re* claim 18, the first alignment feature 82/112 is chosen from one of recesses and projections.

*In re* claim 19, the first device 108 is mounted in a trench 104 in the first surface 102 of the first substrate 100 as seen in Fig. 1.

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*In re* claim 21, first surface 102 comprises a first alignment feature 112 and wherein the second surface 108 comprises a second alignment feature 138/140 complementary to the first alignment feature.

*In re* claim 22, the recess 82 includes a spacer 188/192 as seen in Figures 9 and 10.

*In re* claim 23, wherein the second substrate 10 comprises a plurality of recesses (82, 84, 86), wherein each of the plurality of recesses (82, 84, 86) comprises an alignment feature 138/140 and a device 230/240, and wherein the surface geometry of each of the plurality of recesses (82, 84, 86) is complementary to a first surface of a plurality of further substrates 100, wherein each of the plurality of further substrates 100 comprises an alignment feature 112 and a device 108 chosen from photonic devices, electrical devices, and mechanical devices, such that contacting the alignment feature 112 of each of the plurality of further substrates 100 to the alignment features of each of the plurality of recesses (82, 84, 86) permits each of the further substrates 100 to fit into each of the plurality of recesses (82, 84, 86) thereby permitting the devices 230/240 of the plurality of recesses (82, 84, 86) to be aligned with each of the plurality of devices 108 of the plurality of further substrates 100.

**9. Claims 1-22 and 24-39 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Patent No. US 7,046,868 B2 to Terashima et al. ("Terashima").**

*In re* claims 1-6, 28, 29, and 32, Terashima discloses an optical assembly (Figures 4-17) comprising:

a first photonic/electronic/mechanical substrate/chip/chip sub-mount 10/20/30 comprising a first surface comprising at least a first structure 11/18/19/21/22/31/33 and at least a first alignment feature/device 11/18/19/21/22/31/33;

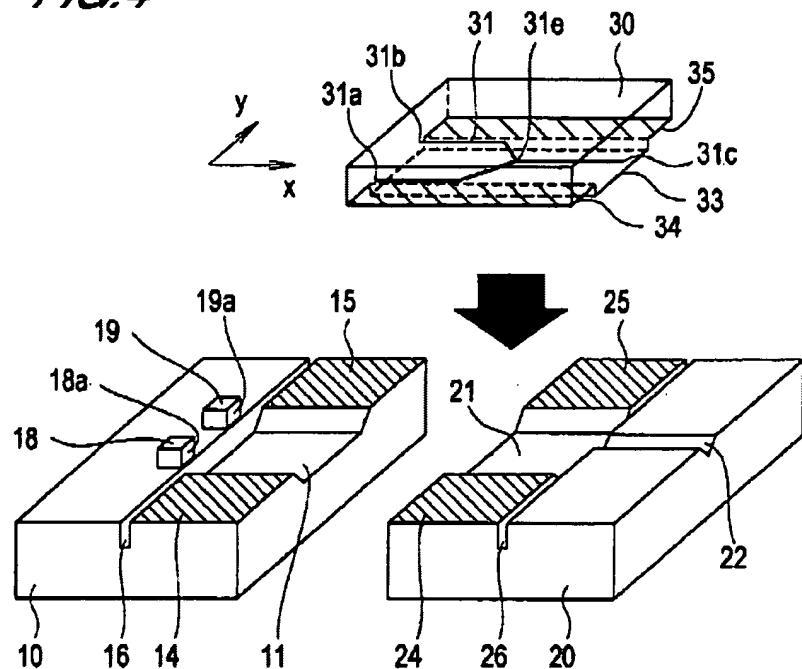
a second photonic/electronic/mechanical substrate/chip/chip sub-mount 10/20/30 comprising a first surface comprising at least a second structure 11/18/19/21/22/31/33 complementary to each of the at least first structure 11/18/19/21/22/31/33 and at least a second alignment feature/device 11/18/19/21/22/31/33 complementary to each of the at least first alignment features 11/18/19/21/22/31/33; and

a device 16/18/19/31/32/52 mounted to at least one of the first surface of the first substrate 10/20/30 and the first surface of the second substrates 10/20/30, the device 16/18/19/31/32/52 selected from one of a photonic device, an electrical device, and a mechanical device;

wherein the first surface of the first substrate 10/20/30 is in physical contact with the first surface of the second substrate 10/20/30 such that each of the first alignment features 11/18/19/21/22/31/33 and each of the corresponding second alignment features 11/18/19/21/22/31/33 are in contact thereby permitting each of the at least first structures 11/18/19/21/22/31/33 to be physically aligned with each of the corresponding complementary at least second structures 11/18/19/21/22/31/33;

wherein the first substrate/chip/chip sub-mount 10/20/30 secures together with the second substrate/chip/chip sub-mount 10/20/30. Figure 4 of Terashima is reproduced below.

*FIG. 4*



*In re* claims 7, 8, 30, 31, and 36, Terashima discloses the particular limitations at column 7, line 2-44.

*In re* claims 9-12, Terashima further discloses v-shaped trenches 22 and a photonic device 52 as claimed.

*In re* claim 13, one of the at least first structures comprises a first trench 22, and wherein a first photonic device 52 is disposed in the first trench 22, and wherein the second substrate 30 comprises a second groove/trench (column 9, lines 4-8), and wherein the device 32 is disposed in the second trench, such that when the chip 20 or 30 and the chip sub-mount 30 or 20 are secured together, the photonic device 52 disposed in the first trench 22 is aligned with device 32 disposed in the second trench.

*In re* claim 14, the recited limitations are clearly shown Figure 4 or 5 of Terashima.

*In re* claim 15, Terashima shows a plurality of photonic chips 102, 104 secured to chip sub-mount 100 in Fig. 17.

*In re* claim 16, the first substrate 10 comprises a plurality of chips (18, 19) and the second substrate 30 comprises a plurality of chip sub-mounts (34, 35) as seen in Fig. 4.

*In re* claims 17-22 and 24-27, the recited limitations are also clearly shown in Figure 5, 6 and/or 17 of Terashima.

*In re* claim 33, the recited limitations are disclosed by Terashima at column 8, lines 1-11.

*In re* claims 34-39, the recited limitations are disclosed by Terashima at column 6, line 51 to column 7, line 41. Note that the multiple etching steps disclosed by Terashima can be considered a form of replicating or direct machining and the dicing disclosed by Terashima can be considered a form of cutting.

### ***Conclusion***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The additional documents cited on the attached form PTO-892 include prior art that

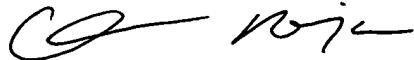
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could also have been used to reject at least one or more the pending claims but were not considered at this time to be more relevant than the patents cited above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Omar Rojas whose telephone number is (571) 272-2357. The examiner can normally be reached on Monday-Friday (9:00PM-5:00PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rod Bovernick, can be reached on (571) 272-2344. The official facsimile number for regular and After Final communications is (571) 273-8300. The examiner's RightFAX number is (571) 273-2357.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Omar Rojas  
Patent Examiner  
Art Unit 2874

or

April 2, 2007



Rodney Bovernick  
Supervisory Patent Examiner  
Technology Center 2800